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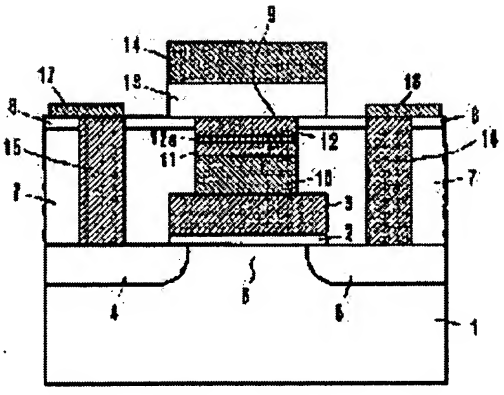
(54) DIELECTRIC DEVICE

(57)Abstract:

PROBLEM TO BE SOLVED: To provide a dielectric device which is superior in polarization characteristic, enhanced in productivity, and reduced in manufacturing cost.

SOLUTION: A source region 4 and a drain region 5 are formed on the surface of a silicon substrate 1, and a gate-insulating film 2 and a gate electrode are successively formed on a channel region between the source region 4 and the drain region 5. An interlayered insulating film 7 is formed on the silicon substrate 1, so as to cover the gate electrode 3 and the gate-insulating film 2, and a contact hole 9 is bored in the interlayered insulating film 7 on the gate electrode 3. A connecting layer 10 and a lower electrode 12 of Bi2Sr2CuO6 are formed inside the contact hole 9. A ferroelectric film 13 of SrBi2Ta2O9 and an upper electrode 14 of Bi2Sr2CuO6 are successively formed on the interlayered insulating film 7, coming into contact with the upside of the lower electrode 12.



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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the dielectric element which has a dielectric film.
[0002]
[Description of the Prior Art] The memory in which the capacitor (it is hereafter called a ferroelectric capacitor) which becomes the gate part of a field-effect transistor (FET) from the ferroelectric film was formed is known as nonvolatile memory in which destructive read is possible. As structure of such ferroelectric memory, MFS (metal, ferroelectric, and semi-conductor) structure, MFIS (metal, ferroelectric, insulator, and semi-conductor) structure, MFMIS (metal, ferroelectric, metal, insulator, and semi-conductor) structure, etc. are proposed.
[0003] Drawing 12 is the typical sectional view showing an example of the ferroelectric random-access memory of MFMIS structure. The ferroelectric random-access memory of drawing 12 is indicated by JP,5-327062,A.
[0004] It sets to drawing 12 and is n+. Predetermined spacing is separated on the front face of a silicon substrate 31, and it is p+. The source field 34 and p+ which consist of a layer The drain field 35 which consists of a layer is formed. The field of the silicon substrate 31 between the source field 34 and the drain field 35 turns into the channel field 36. Gate dielectric film 32 is formed on the channel field 36, and the gate electrode 33 is formed on gate dielectric film 32.
[0005] The interlayer insulation film 37 is formed on the silicon substrate 31 and the gate electrode 33. The contact hole 39 is formed in the interlayer insulation film 37 on the gate electrode 33, and the wiring layer 40 is formed in the contact hole 39.
[0006] A contact hole is prepared in the interlayer insulation film 37 on the source field 34 and the drain field 35, respectively, and wiring layers 45 and 46 are formed in those contact holes, respectively. Furthermore, the lower electrode 42 is formed on the wiring layer 40 connected to the gate electrode 33. The ferroelectric film 43 is formed on the lower electrode 42, and the up electrode 44 is formed on the ferroelectric film 43. Moreover, the ohmic electrodes 47 and 48 are formed, respectively on the wiring layer 45 connected to the source field 34 and the drain field 35, and 46.
[0007] In this ferroelectric random-access memory, the lower electrode 42, the ferroelectric film 43, and the up electrode 44 constitute a ferroelectric capacitor.
[0008]
[Problem(s) to be Solved by the Invention] In the ferroelectric random-access memory of drawing 12 , the lower electrode 42 and the up electrode 44 are usually formed with reactant low metals, such as Pt (platinum). Thus, since it is formed on the lower electrode 42 with which the ferroelectric film 43 consists of a reactant low metal and the interlayer insulation film 37 is formed in the perimeter of the wiring layer 40 between the gate electrode 33 and the lower electrode 42, the reaction and counter diffusion of a configuration atom between the ferroelectric film 43 and a silicon substrate 31 are fully prevented.
[0009] However, in manufacture of the above-mentioned conventional ferroelectric random-access

memory, if it heat-treats at a process after formation of a ferroelectric capacitor, the grain boundary set to Pt which is the ingredient of the lower electrode 42 and the up electrode 44 from a cylindrical crystal will be formed, and the oxygen in the ferroelectric film 43 will become easy to diffuse the inside of Pt. An oxidizing zone is formed by that cause near the interface of the wiring layer 40 which touches the ferroelectric film 43, and resistance of a wiring layer 40 increases.

[0010] Moreover, when a ferroelectric capacitor is placed into the ambient atmosphere containing hydrogen at the time of formation of the insulator layer of a back process, the desorption of the oxygen from the ferroelectric film 43 is promoted by the catalysis of Pt. Thereby, a degradation layer is formed near the interface of the ferroelectric film 43 which touches the up electrode 44. The polarization property of the ferroelectric film 43 deteriorates these results.

[0011] Moreover, reactivity is low, since Pt which is the ingredient of the lower electrode 42 and the up electrode 44 has a difficulty etching property, it requires time amount for processing and productivity is low [Pt]. Furthermore, since Pt is expensive, ingredient cost reaches and a manufacturing cost becomes high.

[0012] The purpose of this invention is having a good polarization property and offering the dielectric element in which the improvement in productivity and reduction-izing of cost are possible.

[0013]

[The means for solving a technical problem and an effect of the invention]

(1) The dielectric element concerning the 1st invention invention of the 1st has the laminated structure of the 1st electrode layer which has the similar crystal structure mutually, and a dielectric film.

[0014] In the dielectric element concerning this invention, the 1st electrode layer and dielectric film have the similarity of the crystal structure. Since the grid adjustment of the 1st electrode layer and a dielectric film becomes good by this, the crystallinity of the dielectric film formed on the 1st electrode layer becomes good, and the interface stability of the 1st electrode layer and a dielectric film improves. Therefore, the dielectric element which has a good component property is realized.

[0015] (2) The dielectric element concerning the 2nd invention invention of the 2nd is characterized by having the 2nd electrode layer in which a laminated structure has the crystal structure still more similar to the 1st electrode layer and a dielectric film in the configuration of the dielectric element concerning the 1st invention.

[0016] In the dielectric element concerning this invention, the 1st electrode layer, a dielectric film, and the 2nd electrode layer have the similarity of the crystal structure. Since the grid adjustment of the 1st electrode layer and a dielectric film and the grid adjustment of a dielectric film and the 2nd electrode layer become good by this, the crystallinity of the dielectric film formed on the 1st electrode layer becomes good, and the interface stability of the 1st electrode layer and a dielectric film and the interface stability of a dielectric film and the 2nd electrode layer improve. Therefore, the dielectric element which has a good component property is realized.

[0017] (3) The dielectric element concerning the 3rd invention invention of the 3rd is characterized by an electrode layer consisting of a conductive oxide in the configuration of the dielectric element concerning the 1st or 2nd invention.

[0018] In this case, the problem of the desorption of the configuration element (for example, oxygen) of the dielectric film by the catalysis of an electrode layer does not arise. Thereby, a good polarization property is acquired in a dielectric film. Therefore, the dielectric element which has a still better component property is realized.

[0019] (4) The dielectric element concerning the 4th invention invention of the 4th is characterized by the crystal structure of an electrode layer and a dielectric film being perovskite type structure in the configuration of the dielectric element concerning the 1st - one of invention of the 3rd.

[0020] In this case, both an electrode layer and a dielectric film have perovskite type structure, and have the similarity of the crystal structure. Since the grid adjustment of an electrode layer and a dielectric film becomes good by this, the crystallinity of the dielectric film formed on an electrode layer becomes good, and the interface stability of an electrode layer and a dielectric film improves.

[0021] Moreover, the electrode layer which has perovskite type structure is easy to process it, and it is

also possible to form according to a continuous process within the same manufacturing installation as the dielectric film which has perovskite type structure. Moreover, the electrode layer which has perovskite type structure can be cheaply formed compared with the metal of a platinum group.
[0022] Therefore, it has a good component property and the dielectric element in which the improvement in productivity and reduction-izing of cost are possible is realized.
[0023] (5) The dielectric element concerning the 5th invention invention of the 5th The 1st and 2nd impurity ranges formed in the semi-conductor substrate or the semi-conductor layer by separating predetermined spacing, The gate dielectric film formed on the field between the 1st and 2nd impurity ranges, The gate electrode formed on gate dielectric film, and the interlayer insulation film which is formed on a semi-conductor substrate or a semi-conductor layer so that a gate electrode and gate dielectric film may be covered, and has a contact hole, The lower electrode layer which is formed in the contact hole of an interlayer insulation film, and is electrically connected to a gate electrode, The dielectric film formed on the interlayer insulation film so that the top face of a lower electrode layer might be contacted, It has the up electrode layer formed on the dielectric film, a lower electrode layer and an up electrode layer consist of conductive oxide which has perovskite type structure, and a dielectric film consists of a dielectric which has perovskite type structure.
[0024] In the dielectric element concerning this invention, a lower electrode layer, an up electrode layer, and a dielectric film have perovskite type structure, and have the similarity of the crystal structure. Since the grid adjustment of a lower electrode layer and a dielectric film and the grid adjustment of a dielectric film and an up electrode layer become good by this, the crystallinity of the dielectric film formed on a lower electrode layer becomes good, and the interface stability of a lower electrode layer and a dielectric film and the interface stability of a dielectric film and an up electrode layer improve. Moreover, the problem of the desorption of the configuration element (for example, oxygen) of the dielectric film by the catalysis of a lower electrode layer and an up electrode layer is not produced, either. Therefore, a good polarization property is acquired in a dielectric film.
[0025] Moreover, the conductive oxide which has perovskite type structure is easy to process it, and it is also possible to form according to a continuous process within the same manufacturing installation as the dielectric film which has perovskite type structure. Furthermore, the conductive oxide which has perovskite type structure can be cheaply formed compared with the metal of a platinum group.
[0026] Since the lower electrode layer which contacts the inferior surface of tongue of a dielectric film especially is prepared in the contact hole of an interlayer insulation film, in case patterning of an up electrode layer and the dielectric film is carried out, the ingredient of a lower electrode layer does not adhere or accumulate on the side attachment wall of a dielectric film. Moreover, since the lower electrode layer is prepared in the contact hole of an interlayer insulation film even when the ingredient of an up electrode layer adhered or accumulates on the side attachment wall of a dielectric film even if, leak of a current does not arise between an up electrode layer and a lower electrode layer. Therefore, the fall of the dependability by adhesion or deposition of the conductive ingredient to the side attachment wall of a dielectric film and the yield is prevented.
[0027] Therefore, it has a good component property and dielectric memory in which the improvement in productivity and reduction-izing of cost are possible is realized.
[0028] (6) In the configuration of the dielectric element concerning the 5th invention, the dielectric element concerning the 6th invention invention of the 6th is formed in the bottom of the lower electrode layer in a contact hole, and is further equipped with the connection layer which connects a lower electrode layer to a gate electrode electrically.
[0029] In this case, a connection layer and a lower electrode layer are prepared in the contact hole of an interlayer insulation film, and the lower electrode layer in a contact hole is electrically connected to a gate electrode by the connection layer.
[0030] (7) The dielectric element concerning the 7th invention invention of the 7th is characterized by for an electrode layer consisting of a stratified conductivity oxide, and a dielectric film consisting of a stratified dielectric in the configuration of the dielectric element concerning the 1st - one of invention of the 6th.

[0031] In this case, since both an electrode layer and a dielectric film have the layer structure, the grid adjustment of an electrode layer and a dielectric film becomes still better. The crystallinity of the dielectric film formed on an electrode layer becomes still better by that cause, and the interface stability of an electrode layer and a dielectric film improves further. Therefore, a still better polarization property is acquired in a dielectric film.
[0032] (8) The dielectric element concerning the 8th invention invention of the 8th is characterized by for an electrode layer consisting of bismuth system stratified conductivity oxide, and a dielectric film consisting of a stratified dielectric containing a bismuth in the configuration of the dielectric element concerning the 1st - one of invention of the 7th.
[0033] In this case, since both an electrode layer and a dielectric film have the layer structure and contain a bismuth, an electrode layer and a dielectric film have the similarity of the crystal structure, and the similarity of a configuration element. Therefore, while the grid adjustment of an electrode layer and a dielectric film becomes still better, formation of the degradation layer by the counter diffusion of a configuration element does not take place between an electrode layer and a dielectric film. The crystallinity of the dielectric film formed on an electrode layer becomes still better by that cause, and the interface stability of an electrode layer and a dielectric film improves further. Therefore, a still better polarization property is acquired in a dielectric film.
[0034] (9) The dielectric element concerning the 9th invention invention of the 9th is characterized by a dielectric film consisting of a ferroelectric in the configuration of the dielectric element concerning the 1st - one of invention of the 8th. In this case, it has a good component property and the ferroelectric component in which the improvement in productivity and reduction-izing of cost are possible is realized.

[0035] (10) The dielectric element concerning the 10th invention invention of the 10th is characterized by for an electrode layer consisting of stratified conductivity oxide containing a bismuth, strontium, copper, and oxygen, and a dielectric film consisting of a stratified ferroelectric containing strontium, a bismuth, a tantalum, and oxygen in the configuration of the dielectric element concerning the 1st - one of invention of the 9th.
[0036] In this case, since both an electrode layer and a dielectric film have the layer structure and contain a bismuth, strontium, and oxygen, an electrode layer and a dielectric film have the similarity of the crystal structure, and the similarity of a configuration element. Therefore, while the grid adjustment of an electrode layer and a dielectric film becomes still better, formation of the degradation layer by the counter diffusion of a configuration element is not performed between an electrode layer and a dielectric film. The crystallinity of the dielectric film formed on an electrode layer becomes still better by that cause, and the interface stability of an electrode layer and a dielectric film improves further. Therefore, it has a still better component property and the ferroelectric component in which the improvement in productivity and reduction-izing of cost are possible is realized.
[0037]
[Embodiment of the Invention]
(1) The 1st example drawing 1 is the typical sectional view showing the structure of the ferroelectric random-access memory in the 1st example of this invention.
[0038] In drawing 1 , predetermined spacing is separated on the front face of p mold single crystal silicon substrate 1, and it is n+. The source field 4 and n+ which consist of a layer The drain field 5 which consists of a layer is formed. The field of the silicon substrate 1 between the source field 4 and the drain field 5 turns into the channel field 6.
[0039] the channel field 6 top -- SiO2 from -- the becoming gate dielectric film 2 is formed. On gate dielectric film 2, the gate electrode 3 which consists of polish recon is formed. The interlayer insulation film 7 is formed on the silicon substrate 1 so that the gate electrode 3 and gate dielectric film 2 may be covered. On the interlayer insulation film 7, the buffer layer 8 which consists of TiO2 (titanium oxide), CeO2, etc. (cerium oxide) is formed.
[0040] The contact hole 9 is formed in the interlayer insulation film 7 and buffer layer 8 on the gate electrode 3. In the contact hole 9, the connection layer (plug) 10 which consists of conductive

ingredients, such as polish recon and W (tungsten), is formed by predetermined Mr. Fukashi.
[0041] On the connection layer 10 in the contact hole 9, the diffusion barrier layer 11 which consists of conductive ingredients, such as TiN and TaSiN, is formed, and Pt layer 12a is formed on the diffusion barrier layer 11.
[0042] On Pt layer 12a in the contact hole 9, the lower electrode 12 which consists of Bi2 Sr2 CuO6 which is Bi (bismuth) system conductivity oxide (BSCO) is formed. The ferroelectric film 13 which consists of SrBi2 Ta 2O9 which has the perovskite mold crystal structure, and which is a stratified ferroelectric (SBT) is formed on the buffer layer 8 so that the top face of the lower electrode 12 may be contacted. Bi2 Sr2 CuO6 which is Bi system conductivity oxide on the ferroelectric film 13 from -- the becoming up electrode 14 is formed.
[0043] A contact hole is formed in the buffer layer 8 and interlayer insulation film 7 on the source field 4 and the drain field 5, respectively, and the source electrode 15 and the drain electrode 16 which consist of conductive ingredients, such as polish recon, are formed in those contact holes, respectively. On the source electrode 15 and the drain electrode 16, wiring layers 17 and 18 are formed, respectively.
[0044] The lower electrode 12, the ferroelectric film 13, and the up electrode 14 constitute a ferroelectric capacitor from ferroelectric random-access memory of drawing 1 .
[0045] In this example, the lower electrode 12 is equivalent to a lower electrode layer or the 1st conductive layer, and the up electrode 14 is equivalent to an up electrode layer or the 2nd conductive layer.
[0046] Drawing 2 is Bi2 Sr2 CuO6 which is the ingredient of the lower electrode 12 of the ferroelectric random-access memory of drawing 1 , and the up electrode 14. It is the mimetic diagram showing the crystal structure. Moreover, drawing 3 is SrBi2 Ta 2O9 which is the ingredient of the ferroelectric film 13 of the ferroelectric random-access memory of drawing 1 . It is the mimetic diagram showing the crystal structure.
[0047] As shown in drawing 2 , it is Bi2 Sr2 CuO6. It is the conductive oxide of the shape of a layer which has the perovskite mold crystal structure. This Bi2 Sr2 CuO6 It can form at about 600 degrees C, low temperature shows a superconductivity, and the specific resistance in a room temperature is about 10-4ohmcm. On the other hand, as shown in drawing 3 , it is SrBi2 Ta 2O9. It is the stratified ferroelectric which has the perovskite mold crystal structure. Bi2 Sr2 CuO6 And SrBi2 Ta 2O9 Both the lattice constants within a field are 0.39nm. Thus, Bi2 Sr2 CuO6 of drawing 2 And SrBi2 Ta 2O9 of drawing 3 It has the similarity of the crystal structure.
[0048] Therefore, the grid adjustment of the lower electrode 12 and the ferroelectric film 13 and the grid adjustment of the ferroelectric film 13 and the up electrode 14 become good. Moreover, the crystallinity of the ferroelectric film 13 formed on the lower electrode 12 becomes good.
[0049] Moreover, as shown in drawing 2 , it is Bi2 Sr2 CuO6. Configuration elements are Sr, Bi, Cu, and O. On the other hand, as shown in drawing 3 , it is SrBi2 Ta 2O9. Configuration elements are Sr, Bi, Ta, and O. Thus, Bi2 Sr2 CuO6 of drawing 2 and SrBi2 Ta 2O9 of drawing 3 It has the similarity of a configuration element.
[0050] Therefore, the effect by the counter diffusion of the configuration element near the interface of the ferroelectric film 13 and the up electrode 14 near the interface of the lower electrode 12 and the ferroelectric film 13 is small. Namely, when Cu in the lower electrode 12 and the up electrode 14 and Ta in the ferroelectric film 13 carry out counter diffusion, SrBi2 Ta 2O9 which is the ingredient of the ferroelectric film 13 partially near the interface in the lower electrode 12 and the up electrode 14 Bi2 Sr2 CuO6 which it is formed and is the ingredient of the lower electrode 12 and the up electrode 14 partially near the interface in the ferroelectric film 13 It is formed. In this case, the interface of the lower electrode 12 and the ferroelectric film 13 and the interface of the ferroelectric film 13 and the up electrode 14 are only confused slightly, and a degradation layer is not formed in these interfaces.
[0051] Furthermore, since the ferroelectric capacitor which consists of the lower electrode 12, ferroelectric film 13, and an up electrode 14 has all oxide mold laminated structures, interface stability becomes good and the problem of the desorption of the oxygen by the catalysis of Pt is avoided. Moreover, even if degradation of an oxygen deficiency etc. takes place to the ferroelectric film 13, the

property of the lower electrode 12, the ferroelectric film 13, and the up electrode 14 can be recovered by performing heat treatment for filling up oxygen. The ferroelectric capacitor which has the outstanding polarization fatigue property is formed these results.

[0052] Moreover, since it becomes possible to form the lower electrode 12, the ferroelectric film 13, and the up electrode 14 according to a continuous process within the same manufacturing installation, productivity improves. moreover, the lower electrode 12 and the up electrode 14 -- Bi2 Sr2 CuO6 from -- when forming using the becoming 6 inches spatter target, compared with the case where it forms using the 6 inches spatter target which consists of Pt, ingredient cost drops to 1/10. Consequently, the cost of ferroelectric random-access memory is reduced.

[0053] Furthermore, since reactivity is high, Bi2 Sr2 CuO6 which is the ingredient of the lower electrode 12 and the up electrode 14 has good workability, and becomes possible [also etching easily by chemical etching]. Moreover, Cl2 to the etching system of reaction Etching adapting reactivity also becomes possible by introducing HBr. Consequently, an etch rate can be increased. Furthermore, it also becomes possible to etch the lower electrode 12, the ferroelectric film 13, and the up electrode 14 into coincidence. Productivity improves these results.

[0054] Drawing 4 - drawing 8 are the process sectional views showing the manufacture approach of the ferroelectric random-access memory of drawing 1 . first, it is shown in drawing 4 (a) -- as -- the p-type silicon substrate 1 top -- the oxidizing [thermally] method -- SiO2 of 100A of thickness from -- the becoming gate dielectric film 2 is formed and the gate electrode 3 which consists of polish recon of 2000A of thickness with a CVD method (chemical vapor deposition) is formed on gate dielectric film 2.

[0055] Next, as shown in drawing 4 (b), the gate electrode 3 and gate dielectric film 2 of a part except the gate formation field on a silicon substrate 1 are removed using dry processes, such as reactive ion etching or ion milling, and the gate section is formed. And it heat-treats by carrying out the ion implantation of the n mold impurity (n mold dopant) to the front face of a silicon substrate 1, using the gate electrode 3 as an ion notes necessary mask. Thereby, the source field 4 and the drain field 5 which consist of an n mold impurity layer (n+ layer) in self align to the gate dielectric film 2 and the gate electrode 3 on a silicon substrate 1 are formed, respectively. The field of the silicon substrate 1 between the source field 4 and the drain field 5 turns into the channel field 6.

[0056] then, it is shown in drawing 4 (c) -- as -- the gate electrode 3 and gate dielectric film 2 -- a wrap -- like -- a silicon substrate 1 top -- a CVD method etc. -- SiO2 of about 6000A of thickness etc. -- from -- the becoming interlayer insulation film 7 is formed.

[0057] subsequently, it is shown in drawing 5 (d) -- as -- an interlayer insulation film 7 top -- TiO2 and CeO2 etc. -- from -- the buffer layer 8 of 500A of becoming thickness is formed. Then, as shown in drawing 5 (e), the contact hole 9 is formed in the buffer layer 8 and interlayer insulation film 7 on the gate electrode 3 with a lithography technique.

[0058] And as shown in drawing 5 (f), the connection layer 10 which consists of conductive ingredients, such as polish recon and W, is formed in the contact hole 9. In this case, the thickness of the connection layer 10 is set up so that the distance from the upper limit of the contact hole 9 to the top face of the connection layer 10 may become 1500A. As the formation approach of the connection layer 10, after forming a conductive layer all over the interior of the contact hole 9, and a buffer layer 8, the conductive layer on a buffer layer 8 is removed by etching the whole surface.

[0059] Next, as shown in drawing 6 (g), the diffusion barrier layer 11 which benefits antioxidizing of the connection layer 10 and diffusion prevention of the impurity to the gate section from conductive ingredients, such as TiN and TaSiN, by a spatter etc. is formed all over the interior of the contact hole 9, and a buffer layer 8.

[0060] And as shown in drawing 6 (h), while removing the diffusion barrier layer 11 on a buffer layer 8 by etching the whole surface of the diffusion barrier layer 11, etchback of the buffer layer 11 is carried out until the top face of the diffusion barrier layer 11 in the contact hole 9 becomes lower than the top face of a buffer layer 8. In this case, it is BCl3 as etching gas. And Cl2 Using mixed gas, as etching conditions, a RF output is set to 250W and a pressure is set to 2x10-2Torr. in addition, the above-mentioned mixed gas -- Ar and N2 etc. -- other gas may be mixed. Thus, the diffusion barrier layer 11 of

300A of thickness is formed on the connection layer 10 in the contact hole 9.
[0061] Next, Bi2 Sr2 CuO6 formed in the upper part on the diffusion barrier layer 11 on a buffer layer 8 and in the contact hole 9 as shown in drawing 6 (i) Pt film 12a is formed for improvement in crystallinity.
[0062] Then, as shown in drawing 7 (j), while removing Pt layer 12a on a buffer layer 8 by etching the whole surface of Pt layer 12a, etchback of the Pt layer 12a is carried out until the top face of Pt layer 12a in the contact hole 9 becomes lower than the top face of a buffer layer 8. In this case, using Ar as etching gas, as etching conditions, a RF output is set to 300W and a pressure is set to 3x10-3Torr. etching -- as SU -- Cl2, HBr, and BCl3 etc. -- other gas may be used and these mixed gas may be used. Thus, Pt layer of 200A of thickness 12a is formed on the diffusion barrier layer 11 in the contact hole 9.
[0063] subsequently, it is shown in drawing 7 (k) -- as -- the Pt layer 12a top on a buffer layer 8 and in the contact hole 9 -- the sputtering method etc. -- Bi2 Sr2 CuO6 from -- the becoming lower electrode 12 is formed.
[0064] Then, as shown in drawing 7 (l), by carrying out flattening of the lower electrode 12 by etchback or the CMP method (the chemical mechanical grinding method), the lower electrode 12 is formed only in the contact hole 9, and the lower electrode 12 of 1000A of thickness is formed in remnants and the contact hole 9. In this case, using Ar, HBr, etc. as etching gas, as etching conditions, set a RF output to 200-400W, and let a pressure be 1x10-3Torr extent.
[0065] In addition, after forming the diffusion barrier layer 11, Pt layer 12a, and the lower electrode 12 in succession instead of carrying out etchback of the diffusion barrier layer 11 and the Pt layer 12a at the process of drawing 6 (h) and drawing 7 (j), respectively, flattening according the lower electrode 12, Pt layer 12a, and the diffusion barrier layer 11 to etchback or the CMP method may be performed to coincidence.
[0066] next, it is shown in drawing 8 (m) -- as -- a lower electrode 12 and buffer layer 8 top -- the sputtering method etc. -- SrBi2 Ta 2O9 from -- the becoming ferroelectric film 13 of 2000A of thickness is formed. furthermore, it is shown in drawing 8 (n) -- as -- the ferroelectric film 13 top -- the sputtering method etc. -- Bi2 Sr2 CuO6 of 1500A of thickness from -- the becoming up electrode 14 is formed.
[0067] Then, as shown in drawing 8 (o), patterning of the up electrode 14 and the ferroelectric film 13 is carried out by etching. In this case, using Ar, HBr, etc. as etching gas, as etching conditions, consider as the RF outputs 200-400W, and let a pressure be 1x10-3Torr extent.
[0068] At the time of etching, a buffer layer 8 may be etched altogether. The ferroelectric film 13 does not necessarily need to be straddling on the buffer layer 8 that what is necessary is just in contact with the top face of the lower electrode 12.
[0069] Next, as shown in drawing 1 , a contact hole is prepared in the buffer layer 8 and interlayer insulation film 7 on the source electrode 4 and the drain electrode 5, respectively, and the source electrode 15 and the drain electrode 16 which consist of conductive ingredients, such as polish recon, are formed in those contact holes, respectively. Finally, the wiring layers 17 and 18 which consist of aluminum are formed on the source electrode 15 and the drain electrode 16. Thus, the ferroelectric random-access memory of drawing 1 is produced.
[0070] In the ferroelectric random-access memory of this example, since the lower electrode 12 is formed in the contact hole 9 of an interlayer insulation film 7, in case patterning of the up electrode 14 and the ferroelectric film 13 is carried out by etching, the conductive ingredient of the lower electrode 12 does not accumulate on the side attachment wall of the ferroelectric film 13. Therefore, the dependability of the ferroelectric random-access memory by deposition of the conductive ingredient to the side attachment wall of the ferroelectric film 13 and the fall of the yield are fully prevented.
[0071] Moreover, since the ferroelectric film 13 is formed on the interlayer insulation film 7 through the buffer layer 8 at the process of drawing 8 (m), while it is prevented that the stress of the ferroelectric film 13 is eased by the buffer layer 8, and a crack occurs on the ferroelectric film 13, it is prevented that the reaction and counter diffusion of a configuration element happen between the ferroelectric film 13 and an interlayer insulation film 7. Consequently, the dependability and the yield of ferroelectric random-access memory improve further.

[0072] Furthermore, since the interlayer insulation film 7 is formed in the perimeter of the conductive layer 10 between the ferroelectric film 13 and a silicon substrate 1, the reaction and counter diffusion of a configuration element between the ferroelectric film 13 and a silicon substrate 1 are fully prevented.
[0073] Here, the principle of operation of the ferroelectric random-access memory of drawing 1 is explained. In order to make the up electrode 14 carry out polarization reversal of the ferroelectric film 13, sufficient forward electrical potential difference is impressed, and the electrical potential difference of the up electrode 14 is again set to 0. Thereby, an interface with the up electrode 14 of the ferroelectric film 13 is charged in negative, and an interface with the lower electrode 12 is just charged.
[0074] In this case, an interface with the ferroelectric film 13 of the lower electrode 12 is charged in negative, and an interface with the gate dielectric film 2 of the gate electrode 3 is just charged. Consequently, an inversion layer will be formed in the channel field 6 between the source field 4 and the drain field 5, and, as for FET, the electrical potential difference of the up electrode 14 will be in an ON state in spite of 0.
[0075] On the contrary, in order to make the up electrode 14 carry out polarization reversal of the ferroelectric film 13, sufficient negative electrical potential difference is impressed, and the electrical potential difference of the up electrode 14 is again set to 0. Thereby, an interface with the up electrode 14 of the ferroelectric film 13 is just charged, and an interface with the lower electrode 12 is charged in negative.
[0076] In this case, an interface with the ferroelectric film 13 of the lower electrode 12 is just charged, and an interface with the gate dielectric film 2 of the gate electrode 3 is charged in negative. Consequently, an inversion layer will not be formed in the channel field 6 between the source field 4 and the drain field 5, but FET will be in an OFF state.
[0077] Thus, if the ferroelectric film 13 is fully carrying out polarization reversal, even after setting to 0 the electrical potential difference impressed to the up electrode 14, FET can be alternatively made into an ON state or an OFF state. Therefore, it becomes possible by detecting the current between source drains to distinguish data "1" memorized by ferroelectric memory and "0."
[0078] (2) The 2nd example drawing 9 is the typical sectional view showing the structure of the ferroelectric random-access memory of the MFMIS structure in the 2nd example of this invention.
[0079] In drawing 9 , predetermined spacing is separated on the front face of the p-type silicon substrate 21, and it is n+. The source field 22 and n+ which consist of a layer The drain field 23 which consists of a layer is formed. The field of the silicon substrate 21 between the source field 22 and the drain field 23 turns into the channel field 24. On the channel field 24, gate dielectric film 25, the lower electrode 26, the ferroelectric film 27, and the up electrode 28 are formed in order.
[0080] In the ferroelectric random-access memory of drawing 9 , the lower electrode 26, the ferroelectric film 27, and the up electrode 28 constitute a ferroelectric capacitor. the lower electrode 26 and the up electrode 28 -- Bi2 Sr2 CuO6 from -- becoming -- the ferroelectric film 27 -- SrBi2 Ta 2O9 from -- it becomes.
[0081] Also in the ferroelectric random-access memory of this example, it has the outstanding polarization degradation resistance like the ferroelectric random-access memory of the 1st example, and the improvement in productivity and reduction-ization of cost are attained.
[0082] (3) The 3rd example drawing 10 is the typical sectional view showing the structure of the ferroelectric random-access memory of the MFIS structure in the 3rd example of this invention.
[0083] In drawing 10 , predetermined spacing is separated on the front face of the p-type silicon substrate 21, and it is n+. The source field 22 and n+ which consist of a layer The drain field 23 which consists of a layer is formed. The field of the silicon substrate 21 between the source field 22 and the drain field 23 turns into the channel field 24. On the channel field 24, gate dielectric film 25, the ferroelectric film 27, and gate electrode 28a are formed in order.
[0084] In the ferroelectric random-access memory of drawing 10 , the channel field 24 of the p-type silicon substrate 21, gate dielectric film 25, the ferroelectric film 27, and gate electrode 28a constitute a ferroelectric capacitor. the ferroelectric film 27 -- SrBi2 Ta 2O9 from -- becoming -- gate electrode 28a -- Bi2 Sr2 CuO6 from -- it becomes.

[0085] Also in the ferroelectric random-access memory of this example, it has the outstanding polarization degradation resistance like the ferroelectric random-access memory of the 1st example, and the improvement in productivity and reduction-ization of cost are attained.
[0086] (4) The 4th example drawing 11 is the typical sectional view showing the structure of the ferroelectric random-access memory of the MFS structure in the 4th example of this invention.
[0087] In drawing 11 , predetermined spacing is separated on the front face of the p-type silicon substrate 21, and it is n+. The source field 22 and n+ which consist of a layer The drain field 23 which consists of a layer is formed. The field of the silicon substrate 21 between the source field 22 and the drain field 23 turns into the channel field 24. On the channel field 24, the ferroelectric film 27 and gate electrode 28a are formed in order.
[0088] In the ferroelectric random-access memory of drawing 11 , the channel field 24 of the p-type silicon substrate 21, the ferroelectric film 27, and gate electrode 28a constitute a ferroelectric capacitor. the ferroelectric film 27 -- SrBi2 Ta 2O9 from -- becoming -- gate electrode 28a -- Bi2 Sr2 CuO6 from -- it becomes.
[0089] Also in the ferroelectric random-access memory of this example, it has the outstanding polarization degradation resistance like the ferroelectric random-access memory of the 1st example, and the improvement in productivity and reduction-ization of cost are attained.
[0090] (5) Other example this inventions of application are applicable also to the ferroelectric random-access memory which has the structure of drawing 12 . In this case, it is Bi2 Sr2 CuO6 about the lower electrode 42 and the up electrode 44. It forms and is SrBi2 Ta 2O9 about the ferroelectric film 43. It forms.
[0091] (6) As an ingredient of other electrode material lower electrodes 12, 26, and 42, the up electrodes 14, 28, and 44, and gate electrode 28a, the conductive oxide which consists of each following ingredient can be used.
[0092] ** It is perovskite die-materials and A2 B-2 Cn Mn+1 O2n+6n=0, and 1, 2, 3, 4 and 5. A is Tl (thallium), Bi, Mg, or Cu, and B is [calcium and M of Ba and C] Cu(s).
[0093] - Sr, and LaMO3 and (Sr, La) 2-MO4M are Ti, V, Cr, Mn, Fe, Co, nickel, Cu, Ru, or Ir.
[0094] - CaMO3M are V, Cr, Fe, or Ru.
[0095] - Ba(Pb, Bi) O3 and LuNiO3 and LnBa2 Cun On+4-an= -- it is 3 and 4. Ln is Y, La, Pr, Nd, Sm, Eu, Gd, Td, Dy, Ho, Er, Tm, Yb, or Lu.
[0096] - Ba and ABiO3A are K or Rb.
[0097] - They are Sr1+n Cun O2n+1n=1, 2 and 3, and infinity.
[0098] It is desirable to use the perovskite die materials of the above-mentioned **, and it is more desirable to use the perovskite die materials especially shown by A2 B-2 CnMn+1 O2n+6.
[0099] Moreover, the conductive oxide which consists of each following ingredient as an ingredient of the lower electrodes 12, 26, and 42, the up electrodes 14, 28, and 44, and gate electrode 28a can also be used.
[0100] ** ReO3 Die materials and ReO3 ** Mx WO3 Die materials M are H, alkali metal, alkaline earth metal, and Cu, Ag, In, Tl, Sn or Pb.
[0101] The lower electrodes 12, 26, and 42, the up electrodes 14, 28, and 44, and gate electrode 28a may be the multilayer structure of each above-mentioned ingredient.
[0102] (7) As other ferroelectric ingredient ferroelectric film 13, 27, and 43, the ferroelectric which consists of each following ingredient may be used.
[0103] ** Bismuth system stratified ferroelectric 2+(An-1 Bn O3n+1) 2 shown by the following general formula (Bi 2O2) - In addition, A is Sr, calcium, Ba, Pb, Bi, K, or Na, and B is Ti, Ta, Nb, W, or V.
[0104] case [of n= 1]: -- case [of -Bi2 WO6 and Bi2 VO5.5n=2]: -Bi2 O3/SrTa2 O6(SrBi2 Ta 2O9):SBT-Bi2 O3/SrNb 2O6 (SrBi2 Nb 2O9)
In the case of n= 3 : -Bi2 O3 / SrTa2 In the case of Bi2 O3 [O6/BaTiO3 and Bi2 O3/SrTaO6/SrTiO3 and]/Bi2 Ti3 O9(Bi4 Ti 3O12):BITn=4: -Bi2 O3 / Sr3 Ti 4O12 (Sr3 Bi2 Ti 4O15)
- Bi2 O3/Bi2 Ti3 O9/SrTiO3 (SrBi4 Ti 4O15)
Although it is desirable as an ingredient of the ferroelectric film 13, 27, and 43 to use the bismuth

system stratified ferroelectric of the above-mentioned **, the ferroelectric which consists of each following ingredient can also be used.

[0105] ** The ferroelectric shown by the following general formula (isotropic ingredient system) - Pb(ZrX Ti1-X) O3-LZT and (Sr1-X CaX) TiO3- ZT(PbZr0.5 Ti0.5) O3 (Pb1-Y LaY) (ZrX Ti1-X) and O3 () :P [Sr1-X BaX] TiO3 : (Sr0.4 Ba0.6) TiO3 and (Sr1-X-Y BaX MY) Ti1-Z NZ O3, in addition M are La, Bi, Sb, or Y, and N is Nb, V, Ta, Mo, or W.

[0106] - As the formation approach of the formation approach ferroelectric film 13, 27, and 43 of Sr2 Nb2 O7 and Sr2 Ta 2O7, and the Pb5 germanium3 O11 and (Pb, calcium) the TiO3(8) ferroelectric film A molecular beam epitaxy method (MBE law), the laser ablation method, a laser molecular beam epitaxy method, the sputtering method (RF mold, DC mold, or ion beam mold), reactant vacuum deposition, and MOCVD -- law (organic metal chemical vapor deposition), the Myst depositing method, a sol gel process, etc. can be used.

[0107] (9) The ingredient of other modification gate electrodes 3 and the connection layer 10 is limited to neither polish recon nor W, but other conductive ingredients may be used for it.

[0108] Moreover, in the above-mentioned example, although FET is formed in silicon substrates 1 and 21, FET may be formed in other semi-conductor substrates or semi-conductor layers.

[0109] In addition, although the above-mentioned example explained the ferroelectric random-access memory which has an n-type channel, the ferroelectric random-access memory which has p mold channel is also realized by making the conductivity type of each class reverse.

[0110] Moreover, this invention is applicable to the various ferroelectric random-access memory which has not only the ferroelectric random-access memory of the above-mentioned example but a ferroelectric capacitor.

[0111] Moreover, although the above-mentioned example explained the case where this invention was applied to the ferroelectric capacitor of the ferroelectric random-access memory which operates as nonvolatile memory, this invention is applicable also to the ferroelectric capacitor of the ferroelectric random-access memory which performs volatile actuation.

[0112] Furthermore, this invention is applicable also to formation of other dielectric elements which have the laminated structure of the dielectric capacitor which has the structure where the dielectric film was inserted by the conductive layer or a dielectric film, and a conductive layer.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the typical sectional view showing the structure of the ferroelectric random-access memory in the 1st example of this invention.
[Drawing 2] Bi2 Sr2 CuO6 which is the ingredient of the lower electrode of the ferroelectric random-access memory of drawing 1 , and an up electrode It is the mimetic diagram showing the crystal structure.
[Drawing 3] SrBi2 Ta 2O9 which is the ingredient of the ferroelectric film of the ferroelectric random-access memory of drawing 1 It is the mimetic diagram showing the crystal structure.
[Drawing 4] It is the process sectional view showing the manufacture approach of the ferroelectric random-access memory of drawing 1 .
[Drawing 5] It is the process sectional view showing the manufacture approach of the ferroelectric random-access memory of drawing 1 .
[Drawing 6] It is the process sectional view showing the manufacture approach of the ferroelectric random-access memory of drawing 1 .
[Drawing 7] It is the process sectional view showing the manufacture approach of the ferroelectric random-access memory of drawing 1 .
[Drawing 8] It is the process sectional view showing the manufacture approach of the ferroelectric random-access memory of drawing 1 .
[Drawing 9] It is the typical sectional view showing the structure of the ferroelectric random-access memory in the 2nd example of this invention.
[Drawing 10] It is the typical sectional view showing the structure of the ferroelectric random-access memory in the 3rd example of this invention.
[Drawing 11] It is the typical sectional view showing the structure of the ferroelectric random-access memory in the 4th example of this invention.
[Drawing 12] It is the typical sectional view showing an example of the conventional ferroelectric random-access memory.
[Description of Notations]
1 21 Silicon substrate
2 25 Gate dielectric film
3 28a Gate electrode
4 22 Source field
5 23 Drain field
6 24 Channel field
7 Interlayer Insulation Film
8 Buffer Layer
9 Contact Hole
10 Connection Layer
11 Diffusion Barrier Layer

12 26 Lower electrode
13 27 Ferroelectric film
14 28 Up electrode

[Translation done.]